SCREEN PRINTED EWT CELLS: LIMITATIONS AND ALTERNATIVE APPROACHES TO THE MANUFACTURING PROCESS

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ABSTRACT: In this paper the influence of the passivation along the pn-junction of a EWT cell is discussed. It can be shown that the surface recombination velocity at the margins of the rear side emitter bordering on the surface of the cell is critical to the cell performance. A processing scheme for the EWT cell is presented using a new masking scheme to define p- and n-type regions on the rear surface. Technical challenges of the metallization process by screen printing are adressed.

Keywords: Back Contact - 1, Manufacturing and Processing – 2, Screen printing - 3

1 INTRODUCTION

The emitter wrap through (EWT) cell concept features two main advantages: due to the absence of a front side metallization the cell does not suffer from shadowing losses. Furthermore, it is particularly suited for mediocre quality substrates as it entails a collecting junction on the front as well as on the rear side of the cell. Since carriers can be collected at both surfaces the EWT cell does not require a high carrier diffusion length in the bulk. EWT cells have been shown to be capable of reaching an efficiency of more than 21% [1].

In order to benefit from these advantages it is however necessary to overcome other drawbacks of the cell design. Due to the necessary interdigitation of the base and emitter electrodes on the rear side, EWT cells typically display an increased area of the pn-junction if compared to conventional cells. Especially, pn-junctions bordering on the surface of the wafer can be particularly harmful if not passivated sufficiently.

We have modelled the influence of such pn-junctions bordering on the surface with regard to the open circuit voltage (V_{OC}) and the fill factor (FF). It can be shown that the recombination velocity at the surface of such junctions is critical and may demand an adaptation in the design of the emitter- and base electrode.

2 MODELING

Kühn et al. [2] have performed two-dimensional modelling of the influence of an open pn-junction bordering on the surface. Using the software DESSIS they have found that a high carrier recombination velocity at the pn-junction in POWER [3] and EWT cells can cause a severe reduction of the fill factor and V_{OC}. Due to the interdigitation of the p- and n-regions on the rear the EWT cell design entails a significant prolongation of the pn-junction bordering on the surface of the wafer. Thus, it is essential that the margins of the n-doped emitter areas on the rear of the cell receive due attention with regard to their passivation.

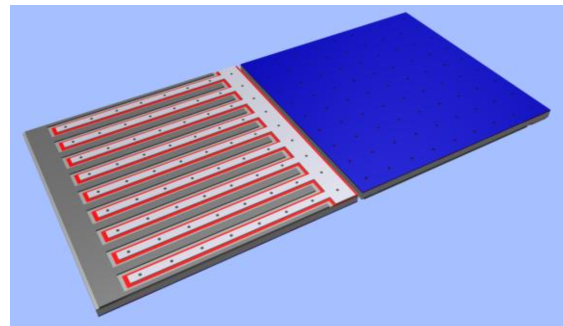

Figure 1: Simplified design of a EWT cell. The cells have a homogeneous front side appearance (right) while the rear side features an interdigitation of both base and emitter regions with their respective electrodes.

Since majority carriers have to drift laterally to reach the interdigitated contacts the total series resistance of the EWT cell is strongly dependent on the wafer resistivity and thickness and therefore the contact pitch. Reducing the pitch in turn leads to further lengthening of the pn-junction. Thus, both base substrate resistivity and the recombination of charge carriers at the pn-junction have to be taken into account when designing emitter and base electrode and determining their pitch.

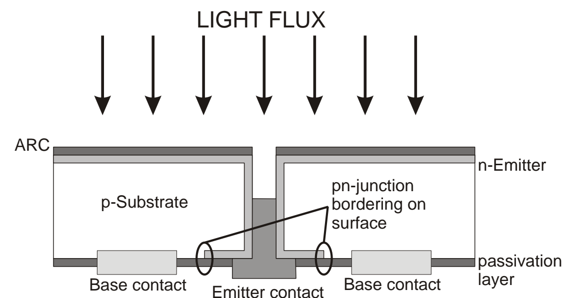

Figure 2: Schematic of an EWT cell. The location of both electrodes on the rear requires p- and n-doped areas, thus prolonging the pn-junction bordering on the rear surface.

Since the EWT cell does not suffer from grid shadowing on the front side and thus benefits from high current densities, the design makes strong demands on the overall series resistance R_s. Calculations suggest a

very narrow pitch of the metallization. Analytical modeling by Neu et al. [4] has shown grid spacing well below 2 mm to be suitable to achieve low ohmic losses comparable to those of conventional cells.

With narrowing of the pitch the effective length per unit area of the pn-juction increases. Kühn et al. [2] have found that the saturation current from the margins of a pn-junction bordering on an unpassivated surface (SRV = 10^7 cm/s) can reach $2{\cdot}10^{-8}$ A/cm. For a pitch of 1.8 mm this would mean a saturation current density J_{02} of approximately $2.6 \cdot 10^{-7}$ A/cm². For a conventional cell this value limits V_{OC} to below 600 mV and pins the fill factor at less than 74% regardless of the series resistance of the cell. Therefore, it is essential to achieve a good surface passivation along the pn-junction.

Depending on the metallization pitch the effective length of the pn-junction of a EWT cell can be up to 40 times that of a conventional cell. A lowering of the surface recombination velocity results in a significant decrease of J_{02} as can be seen in Fig. 3. Dicker et al [5] have found similar dependencies.

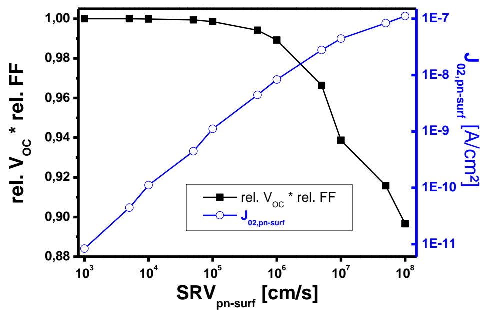

Figure 3: Product of the relative V_{OC} and the relative FF vs. the recombination velocity at the margins of the pn-junction bordering on the surface of the wafer. Additionally, the leakage current density along the pn-junction for a metallization pitch of 1.8 mm is shown.

Neglecting the increased current collection in EWT cells on the rear side of the wafer due to a partial emitter coverage it becomes obvious that in order to achieve an efficiency higher than that of a conventional cell a low SRV at the junction has to be reached. The modeling results suggest that a SRV of 10^7 cm/s may be enough to limit J_{02} to $6{\cdot}10^{-8}$ A/cm². This would suffice to equal the performance of the conventional cell since the current density can be increased by approximately 7% as the EWT cell does not suffer from front grid shadowing.

3 EXPERIMENTAL INVESTIGATIONS

The results show that it is critical to achieve a good surface passivation on the rear of the cell. The passivation has to be applied after defining the p- and n-type regions on the rear and thus has to be suitable for both p- and n-doped surfaces.

As we aim at using a screen printed metallization for both emitter- and base contact the choice for a dielectric coating that is able to maintain its passivating quality in a short high temperature sintering step at this time seems to be limited to thermally grown silicon dioxide (SiO_2).

A simplified processing scheme for a EWT cell with a homogeneous emitter is shown in Fig. 4.

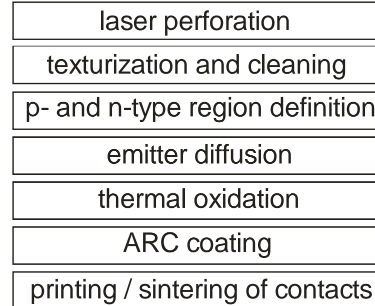

Figure 4: Simplified processing scheme for a EWT cell with screen printed metallization. The method of defining p- and n-type regions is explained below.

One of the most challenging parts of the processing scheme is the partial shielding of the rear side from the emitter diffusion. One of the techniques that has been applied is the use of a diffusion barrier that is screen printed onto the rear side [6]. We have found that this method can lead to shunts on textured surfaces. This is most likely due to local inhomogeneities of the film. The inks that are used do not provide a significant surface passivation leading to increased recombination at the rear. Hacke et al. [7] have added boron to these pastes in an attempt to further improve their passivation quality on p-type substrates.

Another method to avoid the local diffusion of phosphorus into the wafer is shown in Fig. 5.

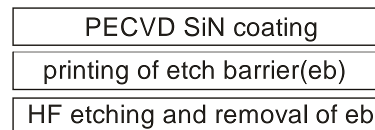

Figure 5: Masking scheme for rear side structuring of p- and n-doped regions. A full area PECVD SiN_x coating is deposited. Afterwards, an etch barrier is screen printed onto the wafer. The areas that are not covered by the barrier are etched in HF and the etch barrier is subsequently stripped from the wafer.

The scheme has two advantages over the conventional screen printable diffusion barrier:

a) The PECVD SiN_x coating allows for the deposition of a homogeneous film. The first experiments have shown that pinholes in the SiN_x layer do not cause shunting even on textured surfaces.

b) The SiN_x coating can be removed together with the PSG etch after the emitter diffusion thus allowing for a good surface passivation in the thermal oxidation afterwards.

The drawback of the method is its higher process cost compared to the screen printed diffusion barrier. An additional PECVD furnace as well as a more complex

wet bench for etching of the SiN_x and stripping of the etch barrier are needed.

4 TECHNOLOGICAL CONSIDERATIONS

The choice of the substrate resistivity and thickness is integral to the development of a suitable electrode design. Although the EWT cell is not affected by wafer warping during the firing process as much as a conventional cell with full area aluminum BSF, it is still desirable to use at least 150 µm thick wafers as the processing sequence entails more processing steps and thus causes increased breakage if particularly thin substrates are used.

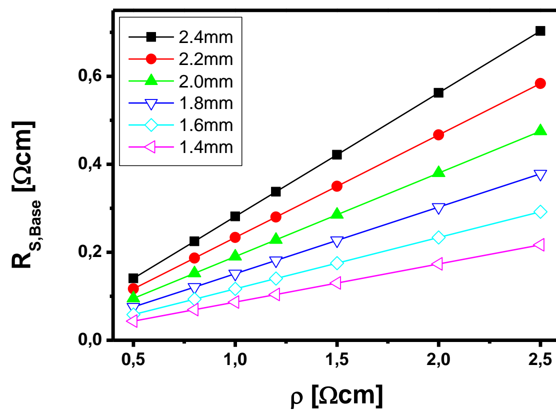

Figure 6: Series resistance contribution of the base substrate vs substrate resistivity for different metallization pitches and a wafer thickness of 150 µm.

It becomes apparent that the EWT concept is suitable only for low resistivity substrates. Using conventional CZ silicon with a resistivity of 4 Ωcm and higher would lead to excessive losses due to the series resistance contribution of majority carriers having to diffuse laterally to the base contact. Of course, a high doping of the base will inevitably give rise to the degradation of the minority carrier lifetime due to the lifetime limiting formation of recombination active B-O-complexes thus causing a drop in V_{OC} and J_{SC}. We expect the decrease of J_{SC} to be less severe though than in conventional cells due to the double sided carrier collection introduced through the rear side emitter [8]. Multicrystalline wafers that usually are more highly doped than CZ wafers and suffer much less from lifetime degradation effects are therefore especially suited for the EWT cell design. On the other hand there are techniques available that might allow the use of low conductivity CZ material without the negative B-O degradation effect in the future [9].

For almost any doping level of the substrate the metallization pitch has to be chosen to be 2 mm or less in order to limit $R_{S,Base}$ to acceptable values. This does not only increase the effective length of the pn-junction but also necessitates the introduction of more holes into the wafer, thus increasing process times and the complexity of suitable laser systems.

To further increase the cell performance it is useful to apply a selective emitter concept to the EWT cell design. A recent development [10] has shown to offer a significant increase in J_{SC} and V_{OC} over a conventional emitter design with high surface doping. The introduction of inkjet printing on the rear side will allow for a minimization of the highly doped area on the rear side.

In order to decrease the manufacturing process complexity it is desirable to find an alternative passivation layer on the rear surface of the cell. A conventional PECVD SiN_x layer seems to be unsuited since the introduced inversion layer below the surface may cause shunting of the p- and n-type regions on the rear.

5 CONCLUSION

It can be shown that the pn-junction on the rear - if not sufficiently passivated - is the dominant source for the losses occurring in screen printed EWT cells. Depending on the effective recombination velocity at the margins of the n-doped regions V_{OC} can drop by as much as 6% and the FF by up to 5% thereby compensating any gain in J_{SC} from the absence of front grid shadowing. To replace the conventional screen printed diffusion barrier for p- and n-type region definition on the rear we have suggested an alternative approach using a dielectric coating. This method has shown to produce reliably good results even on textured surfaces.

The metallization pitch has to be adjusted to the substrate doping and thickness in order to limit the effect of resistive losses from majority carriers diffusing laterally in the bulk.

The implementation of a simple selective emitter design and an alternative passivation layer for the rear surface can significantly increase the cell efficiency and simplify the manufacturing process.

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